AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A system comprising:

a master unit coupled to a slave unit through a request opcode bus, a reply opcode bus and a bi-directional data bus;

wherein the master unit is configured to transfer a last read opcode to the slave unit through the request opcode bus to gain control of the data bus in response to receiving a write request when in a state of not having control of the data bus;

wherein the master unit is configured to take control of the data bus in response to receiving a last read complete token from the slave unit through the reply opcode bus;

wherein the master unit is configured to perform a write operation, corresponding to the write request [[reqeust]], to the [[the]] slave unit through the data bus after taking control of the data bus.

2. (Original) A system comprising:

a master unit coupled to a slave unit through a request opcode bus, a reply opcode bus and a bi-directional data bus;

wherein the slave unit is configured (a) to receive a last read opcode from the master unit through the request opcode bus, (b) to complete pending read requests, in response to receiving the last read opcode, by transferring data corresponding to the read requests to the master unit through the data bus, (c) releasing control of the data bus, and (d) transferring a last read complete token to the master unit.

3. (Original) The system of claim 1 or claim 2, wherein the master unit is a integrated circuit.

4. (Original) The system of claim 1 or claim 2, wherein the slave unit is an integrated circuit.

5. (Original) The system of claim 1 or claim 2, wherein the master unit is a graphics rendering chip.

6. (Original) The system of claim 1 or claim 2, wherein the slave unit couples to one or more memory devices and services transaction requests with respect to the memory devices for the master unit.

7. (Currently Amended) A system for arbitrating control of a data bus, the system comprising:

a request opcode bus;

a reply opcode bus; and

arbitration control logic coupled to a slave unit through the request opcode bus, the reply opcode bus and the data bus, wherein the arbitration control logic is configured to send a first opcode to the slave unit through the request opcode bus in response to (a) receiving a write request from a transfer request buffer and (b) being in an electrically sensing state with respect to said data bus, wherein the arbitration logic is further configured to (c) switch to an electrically driving state with respect to said data bus and (d) write data values, corresponding to the write request, to the slave unit through the data bus in response to receiving a token from the slave unit through the reply opcode bus;

wherein the slave unit is configured to receive the last read opcode, to complete any pending read requests received up to the reception of the last read opcode, and to send a last read complete token to the arbitration control logic through the reply opcode bus.

8. (Cancelled) ~~The system of claim 7, wherein the slave unit is configured to receive the last read opcode, to complete any pending read requests received up to the reception of the last read opcode, and to send a last read complete token to the arbitration control logic through the reply opcode bus.~~